UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/420,887	10/19/1999	PUTHIYA K. NIZAR	042390.P7149	3400

8791 7590 05/27/2004

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD, SEVENTH FLOOR
LOS ANGELES, CA 90025

EXAMINER	
ROBERTSON, DAVID L	
ART UNIT	PAPER NUMBER
2186	15

DATE MAILED: 05/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/420,887	NIZAR ET AL.	
	Examiner	Art Unit	
	David L. Robertson	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This Office action is in response to the RCE and amendment filed March 4, 2004.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 21-23 are rejected under 35 U.S.C. 102(a) as being anticipated by *Intel Offers SDRAM Alternative to Rambus on Camino Chipset* from Computergram International (hereafter Computergram). As was well known, the Camino chipset included a memory controller hub

(i.e., a memory control hub) that included an RDRAM memory channel interface (i.e., a memory channel coupled to the memory control hub). The Computergram reference teaches that "it was previously possible to support SDRAMs through Camino via a converter riser card for RIMM/DIMM memory modules." Note that the riser card inherently includes a memory bus (i.e., through which SDRAM may be accessed) and SDRAM memory (i.e., a memory device coupled to the memory bus), the riser card is inherently understood to receive a memory control packet (i.e., Rambus protocol) and to generate memory control signals on the memory bus. The Rambus protocol includes a Rambus-type bus, which includes separate control and data portions and sends and receives write data packets and read data packets.

Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Ryan (U.S. 6,449,679 B2) in view of the Rambus documents cited in the IDS of August 25, 2003. Note that because Ryan clearly discloses communicating with "a memory controller, intended to directly communicate with a RAMBUS RDRAM memory system" it is appropriate to refer to the noted Rambus documentation for any Rambus or RDRAM particulars that are not explicitly addressed by the Ryan disclosure. Ryan reference teaches a memory control hub that receives a memory control packet (see claim 14, "a memory controller that issues and receives commands in a packet based...protocol"), a translation hub that includes a memory channel interface and a memory bus interface (see claim 14, "a single interface device located between the memory controller and the in-line memory module sockets, the interface device receives and translates packet based...protocol command and data signals;") and generates or places them on the memory bus interface (see claim 14, "translates...into the column/row protocol;" i.e., memory control signals responsive to the memory control packet); the memory bus interface having

memory devices coupled thereto (see claim 14, "a plurality of memory modules each comprising...DRAM devices, the memory modules are located in in-line memory module sockets"). Note that a clock signal 182 is provided to the interface device (translator hub) by a clock source 135 and a copy of this clock signal is also provided to the main memory DIMMs. This clock signal is the signal to which both the memory bridge (memory control hub) and the SDRAM timing is referenced, thus the Ryan system similarly times transmission of the memory control packet based on the memory bus cycle time as claimed by applicants. While not explicitly indicated by the Ryan reference but clearly evident from the Rambus documents of record, the Rambus channel incorporated therein includes a separate control portion and data portion, (e.g., COL and ROW pins and DQA/DQB pins). The Rambus protocol is known to include WR, RD and other commands in COLC packets, mask bits in COLM packets etc., thus these are clearly "memory control packets." The Rambus protocol clearly includes command flag bits in the memory command packets that distinguish between read (RD), write (WR), activate (ACT) and extended (e.g., PRER, REFA, TCAL, etc.) commands. As pointed out by applicants, the Ryan reference additionally teaches transmitting memory row, memory bank and memory column addresses in a combination of ROWx and COLx packets. The examiner's position is that this combination of ROWx and COLx packets constitute the claimed "memory control packet" as needed. Thus, Ryan teaches all of the limitations of applicants' claims.

Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ingenio *et al.* (U.S. 6,041,361). As noted in the previous rejections, the Ingenio reference stands for the proposition of connecting any *known* protocol from a memory controller to any *known* memory device via appropriate translation. Since both SDRAM and Rambus protocols were *known* at the

time of applicant's invention, and further applicants' claims do not distinguish from the conversion of Rambus protocol to SDRAM protocol as noted above, the teachings of Ingenio are appropriately applied to these well known, but otherwise incompatible, memory systems.

Applicants' arguments filed March 4, 2004 have been fully considered but they are not persuasive. Note that upon further investigation, the "*presentation*" reference used in some of the previous Office actions was not submitted in the Ryan application until February 11, 2002, thus its application as prior art is uncertain. Applicants further allege that because the language "'memory control packet' had no generally accepted meaning by those skilled in the art at the time of the invention" and because applicant's specification indicates that applicant's disclosed "memory control packets" differ from the packets of the RDRAM protocol, that the application and the Ryan patent must be patentably distinct. It is the examiner's position, however, that the language "memory control packet" is generic for any type of command sent to a memory system in packet form. Further, there is nothing in the claims that is capable of distinguishing between applicants' claimed "memory control packets" and any other form of command packets sent to a memory. Thus the distinction argued is not persuasive. Applicants additionally argue a timing distinction that has been addressed above. Finally, with respect to the Ingenio rejection, applicants' arguments are laughable. Applicants are required to point out how the claims of the present application distinguish over the applied art; it is irrelevant in this application whether Ryan's claims distinguish or not. Further, applicants' arguments further reinforce the notion that the present claims are not patentably distinct from those of Ryan.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The Electronic Engineering Times reference reports an announcement of an upcoming Intel Rambus to SDRAM translation ASIC.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L. Robertson whose telephone number is (703) 305-3825. The examiner can normally be reached on weekdays from 9 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim, can be reached on 703-305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David L. Robertson
Primary Examiner
Art Unit 2186